Appl. No. 10/715,611
Examiner: PHAM, THANHHA S, Art Unit 2813
In response to the Office Action dated March 8, 2005

Date: June 8, 2005
Attorney Docket No. 10113171

REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Responsive to the Office Action mailed on March 8, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al (US 6,069,038).

In this paper, claims 1 is amended to recite a method of filling a bit line via comprising the step of forming doped conductive layer, lower than the top surface of the gate electrode, overlying the drain region. Claim 11 is amended to recite a method of filling a bit line via comprising the step of etching the doped conductive layer to leave a remaining portion of the doped conductive layer lower than the top surface of the gate electrode. Support for these amendments can be found on page 8, lines 5-8 and Fig. 2H of the application. New claim 20 is added. Support for the new claim can be found in the original claims and Fig. 2G. The specification is amended to improve clarity and further describe features shown in Figs. 2H and 2G. Thus, on entry of this amendment claims 1-20 are pending.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 35 U.S.C. 102(b)

Claims 1-19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

As amended, claims 1 and 11 recite a step of forming or etching a doped conductive layer to produce a doped conductive layer overlying the drain region that is lower than the top surface of

the gate electrode. This unique feature results in a doped conductive layer as bit line contact on a drain region as a dopant source and passivation, avoiding abnormal extension of the drain region and source region, and eliminating unwanted carriers and lattice damage in the exposed drain region. See page 9, lines 3-10 of the specification.

Hashimoto et al do not teach or suggest a method of filling a bit line via comprising the step of forming doped conductive layer, lower than the top surface of the gate electrode, overlying the drain region, as recited in claim 1, or a method of filling a bit line via comprising the step of etching the doped conductive layer to leave a remaining portion of the doped conductive layer lower than the top surface of the gate electrode, as recited in claim 11.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
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> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Hashimoto et al teach a method of manufacturing a semiconductor integrated circuit in which the doped conductive layer overlying the drain region is lower than the dielectric layer, but higher than the top surface of the gate electrode. Specifically, Hashimoto et al teach that plugs 26 overlying the semiconductor regions 11 are lower than silicon nitride film 22 and silicon oxide film 27, but higher than the top surface of the gate electrode 8A. See column 11, line 56 to column 12, line 32 and Figs. 14-16 of Hashimoto et al.

Hashimoto et al do not teach or suggest forming or etching a doped conductive layer such that the doped conductive layer overlying the drain region is lower than the top surface of the gate

electrode, as recited in claims 1 and 11. On the contrary, Hashimoto et al teach the plugs 26 overlying the semiconductor regions 11 are lower than silicon nitride film 22 and silicon oxide film 27, but higher than the top surface of the gate electrode 8A.

It is therefore Applicant's belief that claims 1 and 11 are allowable over the cited reference. Insofar as claims 2-10 and 21-19 depend from claims 1 and 11, respectively, it is Applicant's belief that these claims are also allowable.

New Claim 20

New claim 20 recites a method of filing a bit line contact via further comprising the step of conformally forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region. This unique feature allows for better control the thickness of the doped conductive layer overlying the drain region. See Figs. 2G and 2H.

Hashimoto et al teach the plugs 26 are blanketly formed. Specifically, Hashimoto et al teach the plugs 26 overlying the semiconductor regions 11 fill the openings 24 and 25. See column 12, lines 1-8 and Fig. 14 of Hashimoto et al. A conformally formed layer substantially would extend along the profile of the underlying layers and could not fill the openings.

Hashimoto et al do not teach or suggest conformally forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region. Hashimoto et al only teach the doped conductive layer is blanketly formed to fill the opening in the underlying layer.

For this reason, in addition to the reasons described in connection with claims 1 and 11, it is Applicant's belief that claim 20 is allowable over the cited references.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

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Respectfully submitted,

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